REMARKS

The present communication is filed in response to the final rejection of claims 1, 2, 7-20, 25-38, 41, 43, 46, 48, 49 and 51 in the Office action issued September 5, 2007. Claims 8-18, 25-34, 36, and 38 have previously been withdrawn. Claims 1, 2, 19, 20, 35, 37, 41, 43, 45, 46, 48, 49, and 51 are presently amended. No new matter has been added. Accordingly, claims 1, 2, 7, 19-20, 35, 37, 41, 43, 45-46, 48-49 and 51 remain pending for the Examiner's consideration.

Claim Objections

The Examiner objected to claims 1, 19, 35, 37, 41, 43, 46, and 49 for including informalities. In response to the Examiner's comments, claims 1, 19, 35, 37, 41, 43, 46, and 49 have been amended to cure such informalities. Accordingly, Applicants respectfully request that the objections to claims 1, 19, 35, 37, 41, 43, 46, and 49 be withdrawn.

The Examiner also objected to claims 2, 20, 45, and 48 as being of improper dependent form. Specifically, the Examiner contends that these claims fail to further limit the subject matter of a previous claim. Applicants respectfully disagree.

Each of claims 2, 20, 45, and 48 recites the implementation of a first-in-first-out ("FIFO") memory. Each of claims 2, 20, 45, and 48 further recites that transferring of packets is performed "cluster by cluster." Claim 2, for example, recites the information processing apparatus of claim 1 wherein "said memory means includes an input FIFO, and said transferring of said packets is made cluster by cluster, said cluster being of a predetermined data amount." Claim 1 does not require that the memory include an input FIFO. Clearly such limitation is of a narrower scope. Moreover, claim 1 does not require packet transfers to be performed cluster by cluster.

This limitation is also clearly narrower. Similarly, none of the independent claims from which claims 20, 45, and 48 depend require input FIFO or cluster by cluster packet transfer.

Accordingly, Applicants respectfully submit that claims 2, 20, 45, and 48 are of proper dependent form, and request that the objections to these claims be withdrawn.

Claim Rejections Under 35 U.S.C. § 112, First Paragraph

The Examiner rejected claim 51 under 35 U.S.C. § 112, first paragraph, as lacking enablement. Specifically, the Examiner states that the Specification is enabling for "setting the maximum LBA of the memory area of the transport stream into the register, the LBA can be automatically returned to the start LBA of the memory capacity." (*See 9/5/07 Office Action*, page 3). However, the Examiner states that the Specification does not support claim 51 as previously presented.

Applicants maintain that claim 51 as previously presented is supported in the Specification. Nevertheless, to the extent confusion may have arisen by its previous language, Applicants have amended claim 51 in the interest of clarity. Support for such amendment may be found in the Specification, for example, on page 23, lines 14-27.

Claim Rejections Under 35 U.S.C. § 112, Second Paragraph

The Examiner rejected claims 1, 2, 7, 19, 20, 35, 37 41, 43, 45-46, 48-49, and 51 under 35 U.S.C. § 112, second paragraph as being indefinite.

In response to the Examiner's rejection of claim 1, Applicants have amended claim 1 for clarification. Having addressed all of the limitation indicated by the Examiner as being unclear, Applicants respectfully submit that claim 1 is patentable under § 112, second paragraph, and request withdrawal of this rejection. Applicants have similarly amended claims 19,

35, and 37. Therefore, Applicants submit that claims 19, 35, and 37 are compliant with § 112, second paragraph, and respectfully request that the rejections of these claims also be withdrawn.

Further, Applicants submit that the amendments to claims 1, 19, 35, and 37 render claims 2, 20, 41, 43, 45, 46, 48, and 49 compliant with §112. Accordingly, Applicants request that the §112 rejections of claims 2, 20, 41, 43, 45, 46, 48, and 49 be withdrawn.

The Examiner rejected claim 51 as being indefinite for reciting "wherein in said register the maximum address of the memory in the recording means is set for automatically returning to the start address." In response to this rejection, Applicants have amended claim 51 for clarity. Accordingly, it is respectfully submitted that claim 51 is patentable under § 112, second paragraph, and withdrawal of its rejection is requested.

Claim Rejections Under 35 U.S.C. § 103(a)

The Examiner rejected claims 1, 2, 7, 19-20, 35, 37, 41, 43, 45-46, 48-49 and 51 as being unpatentable over alleged Applicant's admitted prior art ("AAPA": Fig. 1, Specification pages 1-9) in view of U.S. Patent No. 5,881,248 to Mergard ("Mergard").

Independent claim 1 of the present application has been amended to recite:

> "index adding means, residing outside a central processing unit, for adding an address of a sector of a minimum unit of recording on the recording means as an index to said packets read out by said memory control means and for outputting said packets having the added address to said recording means;
>
> an arbiter for mediating said packets extracted by said extracting means and

> stored by said memory means, and for mediating said packets outputted from said memory means to said index adding means in response to an instruction from said memory control means."

Applicants respectfully submit that nothing in the prior art disclosed by Applicants or cited by the Examiner meets these limitations.

The Examiner contends that the "index adding means" limitation is met by AAPA description of a central processing unit ("CPU") 1 and a hard disk interface ("I/F") 24. (*See 9/5/07 Office Action*, page 6). Specifically, the Examiner points to page 8 of the AAPA, where Applicants describe the necessity of the host CPU executing issuance of a command to the hard disk, setting the address at every transfer, and setting the transfer start time. As an initial matter, Applicants would like to point out that no part of the AAPA describes "adding an address of a sector of a minimum unit of recording on the recording means as an index to said packets read out by said memory control means." Accordingly, the entities specified by the Examiner do not meet such limitation. Moreover, Applicants further explain in the Specification that the necessary processes of executing issuance of a command to the hard disk, setting the address at every transfer, and setting the transfer start time become burdensome on the CPU. Thus, Applicants describe a system which functions to shift that burden onto a direct memory access ("DMA") unit. Accordingly, it is clear that index adding means cannot refer to the CPU.

Despite these facts, and in the interest of clarifying the index adding means of claim 1, Applicants have amended the claim to indicate that the index adding means are located outside the CPU. As discussed above, the AAPA does not teach index adding means, or any means for "adding an address of a

sector of a minimum unit of recording on the recording means as an index to said packets read out by said memory control means." Further, Mergard fails to cure this defect.

The Examiner further contends that the "arbiter" recited in claim 1 is taught by AAPA's disclosure of a microcontroller 28. As described in the AAPA, the microcontroller 28 "monitors a status of storage in the input FIFO 23 or an output FIFO 25, and controls the reading and writing operations of data in each FIFO." (*Specification*, page 5, lines 19-23). This is quite different from "mediating said packets outputted from said memory means to said index adding means in response to an instruction from said memory control means" as recited in claim 1. Rather, the microprocessor 28 *is* the memory control means, and so does not receive instructions to mediate from another entity. Nothing in the AAPA, or in Mergard, is equivalent to the arbiter of claim 1.

In light of at least the distinctions described above, Applicants respectfully submit that claim 1 is patentable over AAPA and Mergard, taken alone or in combination. Therefore, withdrawal of the rejection of claim 1 is respectfully requested.

Independent claims 19, 35, and 37 recite limitations similar to those of claim 1, and were rejected on the same bases as claim 1. Moreover, independent claims 19, 35, and 37 have been amended in a manner similar to claim 1. Thus, for at least the reasons discussed above in connection with claim 1, Applicants respectfully submit that claims 19, 35, and 37 are patentable. Further, Applicants request that the rejections of these claims under §103 be withdrawn.

Claims 2, 7, 20, 41, 43, 45-46, 48-49 and 51 depend from one of the independent claims 1, 19, 35, and 37 discussed above. Accordingly, the limitations of the independent claims inhere within corresponding dependent claims. Thus for at least

the reasons discussed above in connection with claims 1, 19, 35, and 37, Applicants respectfully submit that claims 2, 7, 20, 41, 43, 45-46, 48-49 and 51 are also patentable. Accordingly, Applicants request that the rejections of claims 2, 7, 20, 41, 43, 45-46, 48-49 and 51 under §103 be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he/she telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

By _____

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